Radiation Evaluation of An Advanced 64Mb 3.3V DRAM and insights Into the Effects of Scaling on Radiation Hardness

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ABSTRACT

Total ionizing dose radiation evaluations o] a 64Mb DRAM arc presented. The effects of scaling on radiation hardness arc studied utilizing test structures and 16Mb DRAMs with varying feature sires from the same line.

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ABSTRACT

In this paper, total ionizing dose radiation evaluations of a 64Mb 3.3V, fast page mode DRAM and the IBM LUNA-ES 16Mb DRAM arc presented. The effects of scaling on total ionizing dose radiation hardness arc studied utilizing test structures and a series of 16 Mb DRAMs with different feature sires from the same manufacturing line. Excellent agreement was found between the threshold voltage shifts of 16 Mb DRAM test structures and the threshold voltage measured on complete circuits using retention time measurements.

INTRODUCTION

Advances in DRAM density and performance continue to occur. Currently, densities of 1 Gb are being achieved in advanced prototype DRAMs [1-2]. Design rules for these advanced DRAMs arc 0.25 pm or less with sub-micron ccl l areas. As device geometry shrinks radiat ion hardness can bc altered significantly.

In earlier work wc showed that retention time was a useful circuit-level parameter to evaluate total close degradation of DRAMs [3]. Results of the earlier work showed that there was no strong correlation with increased device scaling and radiation tolerance for DRAMs with 0.5 to 0.8 μm feature sizes. However, there was a general trend towards lower total ionizing dose tolerance for devices with reduced supply voltages.

DRAMs continue to gain acceptance for critical space flight applications. Cassini, Mars-Pathfinder, Clemintine, MESUR, and Pluto Express arc examples of current and future space projects that arc either using or exploring the potential for DRAM spacecraft insertion. Application of DRAMs in space is typically in solid state recorders (SSRs), which require large amounts of memory with the lowest power possible.. 'l'his makes the DRAM a natural choice because of their high density and low power consumption.

EXPERIMENTAL APPROACH

Electrical measurements on DRAM circuits were performed with an Al DVANTEST T3342 VI .S1 test system. Test structures were measured with a Hewlett-Packard 4062C semiconductor parametric measurement system. All devices were irradiated with a ^{60}Co room type. irradiator, at 10-65 rad(Si)/sec at room temperature. Source calibration was maintained using a MDI 1 Industries Inc. model 2025AC Radiation Monitor used with the model 20X5-0.6 ion chamber.

While dynamic bias was maintained on all DRAMs tested, automatic in-situ measurements were made on a regular basis of standby supply current, operating supply current, output drive current, and functionality. These measurement were followed by a complete. remote measurement of electrical performance by removing the device under test from the in-situ fixture and inserting it directly onto a second test head. In-situ measurements correlated well with remote measurements in all cases.

Devices used for this work included 16Mb DRAMs, test structures from the 16Mb line, and a 64Mb DRAM.

Test structures were obtained for 16Mb DRAMs from one manufacturer which allowed direct corroboration of the relationship between retention time and threshold voltage which will be discussed in a later section of this paper. A few characteristics of the test structures and the 16Mb DRAM are summarized in "l-able 1 below.

The 3.3V 64Mb DRAM is configured as a 16Meg x 4 bit memory may. This DRAM is fabricated with 0.37 µm design rules and has an 11 nm access transistor gate oxide thickness. Additional device information for the 64Mb DRAM is included in Table I below.

Table 1. Description of Test Devices.

Device Type	Memory Configuration	Access Device Dimensions (W/L)	Cell Area	Gate T_{ox}	Field T_{ox}
16 Mb Test Structures	Not Applicable	0.864/0.675 µm	Not Applicable	15 nm	340 nm
16 Mb DRAM	4 Meg x 4 Bit	0.864/0.675 µm	1.01 µm^2	15 nm	340 nm
64 Mb DRAM	16 Meg x 4 Bit	0.4/0.37 µm	0.156 µm^2.	11 nm	240 nm

EXPERIMENTAL RESULTS

64Mb, 3.3V, Fast Page Mode DRAM

This DRAM, which is a prototype of a new product that is in development was irradiated at 10 rad(Si)/second while dynamically biased, in-situ measurements of dynamic supply current, standby supply current, input leakage current high, and functionality with error count were taken using a 10 foot in-situ cable that allowed full tester capabilities at the device under test.

in Figure 1, standby supply current is plotted as a function of dose. Note that standby current starts out at about 500 µA and increases rapidly to over 4 mA after 15 krad(Si). The device continued to operate at higher levels of radiation and exhibited functional failure at 30 krad(Si). Radiation response of this device was very similar to that of older devices from this manufacturer. Retention time measurements were also mode on this device, and they behaved similarly to older DRAMs. The full paper wiii include additional data which will be. analyzed and compared to other devices.

In previous work [3], wc. noted two distinct classes of supply current degradation. in the first class of degradation a rapid increase in supply current occurs followed by functional failure. Figure 2 shows this type of current degradation. This first class of current degradation is believed to be field oxide inversion which could easily account for the excessive current.

A second type of current degradation can be seen in Figure 2 and that is a more gradual increase with functional failure occurring at substantially higher total doses. The second, more gradual current degradation mode is believed to be caused by threshold voltage shifts in the access device of the memory cell; test structure test data, discussed in a later section, corroborates this assumption.

Retention Time Analysis

DRAM retention time measurements can provide indirect information about *changes* in the threshold voltage of internal transistors provided certain assumptions are valid, namely that the primary source of leakage current in the DRAM storage element is subthreshold leakage in the access transistor. Note that the threshold voltage that applies here corresponds to the very low current region of the device characteristics. With the assumption that leakage current on the DRAM array is dominated by subthreshold leakage, changes in retention time is proportional to current.

Changes in subthreshold current can be related to changes in threshold voltage by the equation:

$$\log\left(\frac{I_2}{I_1}\right) = \frac{m}{2.303}\eta D \qquad (1)$$

where: I_1, I_2=subthreshold current, m=subthreshold slope, η= hole trapping efficiency, anti D=dose in krad(Si).

Which can be expressed in terms of retention time by the following:

$$\log\left(\frac{\tau_2}{\tau_1}\right) = \frac{(3.6 \times 10^{-4}) tox^2}{2.303} m\eta D \qquad (2)$$

where: τ_1, τ_2=retention time (50% level), m=subthreshold slope, η=hole trapping efficiency, D=dose in krad(Si), and *tox* is expressed in nm.

This allows threshold voltage changes due to radiation to be determined from circuit level parameters.

Retention time distributions can also be used to evaluate the distribution of threshold voltages on the entire DRAM array, as well as the uniformity of these distributions after irradiation. For example, the distribution of retention times in Figure 3 corresponds to a standard deviation of approximately 8 mV in threshold voltage assuming that subthreshold leakage is the dominant mechanism. This further corroborates the relationship between retention time and threshold voltage shift in DRAMs. If we assume. that the nominal threshold voltage is 0.7V, this corresponds to a threshold fluctuation of 7 mV for the distribution of devices on the entire chip. This compares closely with calculations of the effect of doping fluctuations on threshold voltage of -t\- 9 mV of 0.6 µm devices from Reference 4. Evaluating the standard deviation of V_T at different radiation levels shows that it is essentially unchanged.

The effective threshold volts.gc can be extracted from the mean value of the normalized retention time, as shown in Figure 4. Note that the slope is nearly constant, which corresponds to the case where oxide traps dominate the threshold voltage response. All three 16Mb devices have similar slopes, and correspond to about 109'o hole trapping for oxide thicknesses of 15 nm. The test structure data available for one of the device types provides a direct check on the validity of this approach. As shown in Figure 5, the. threshold voltage slope is linear with dose. It is only at the highest dose of 55 krad(Si) that field oxide leakage occurs and distorts the subthreshold characteristics and can be seen in Figure 5 as an anomalous increase in ΔV_{TI} between 45 and 55 krad(Si).

Figure 6 shows a subthreshold plot for the 16Mb 5V/3.6V process test structure. Transistor dimensions are: 0.864/0.675 µm. Note the large current increase at the highest dose of SS krad(Si). This is due to field oxide leakage in the device and is also indicated as increased ΔV_{TI} in Figure 5.

SUMMARY

Total ionizing dose data have been presented for the first time for a 64Mb 3.3V DRAM. A new method of measuring individual cell response to ionizing radiation using retention time was shown to correlate very well with threshold voltage data taken from test structures from the same 16Mb DRAM process.

The full paper will include data taken from DRAMs using, test modes that allow special operation of the device. These data will yield additional insight into the effects of ionizing radiation on highly scaled devices.

REFERENCES

[1] M. Horiguchi, et. al, "An Experimental 220MHz 1Gb DRAM," to be presented at the 1995 IEEE International Solid-State Circuits Conference, February 17, 1995.

[2] T. Sugibayashi, et. al, "A 1 Gb DRAM for File Applications," to be presented at the 1995 IEEE international Solid-State Circuits Conference, February 17, 1995.

[3] D.C. Shaw, G.M. Swift and A.H. Johnston, "Radiation Effects in 1 ive Volt and Advanced Lower Voltage DRAMs," IEEE Trans. Nucl. Sci., NS-41, 2452-2458 (1994).

[4] K. Nishinohara, N. Shigyo and T. Wada, IEEE Trans. Elect. Dev., ED-39, 634 (1992)

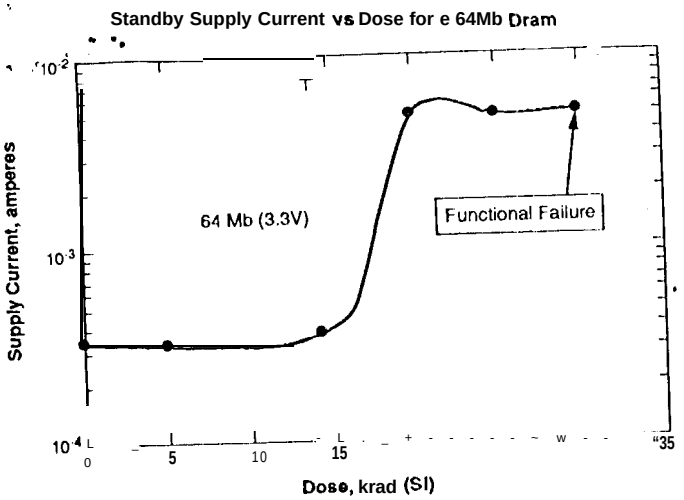

Figure 1. Standby Supply Current vs. Dose for a 64Mb DRAM Note the rapid onset of current after 15 krad(Si).

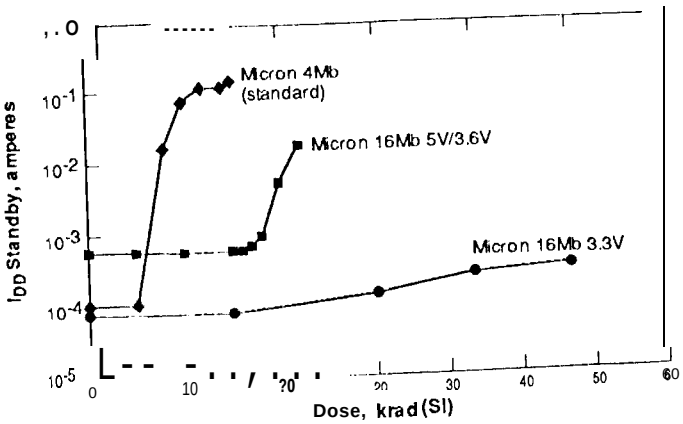

Figure 2. Supply current vs. dose for three 16Mb DRAMs. Note the differing leakage mechanisms for each device.

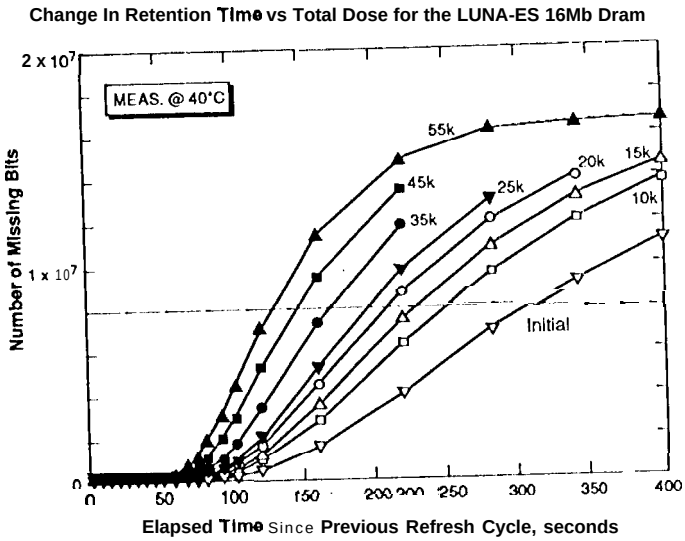

Figure 3. Retention time. curves for the IBM LUNA-ES 16Mb DRAM, with dose as a parameter.

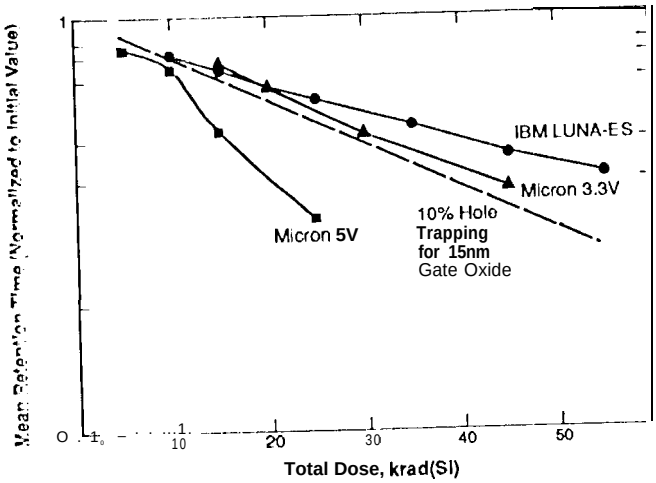

Figure 4. Mean normalized retention time vs. dose for sever-al 1 DRAMs. Note the decreased hole trapping indicated by reduced slope for each DRAM as scaling increases.

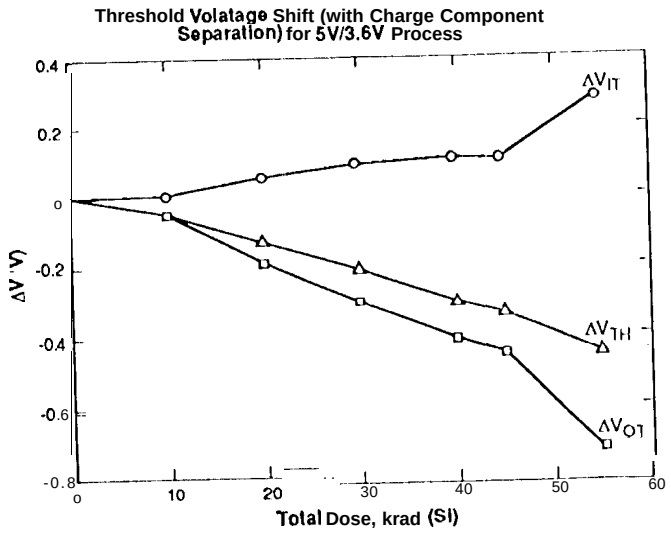

Figure 5. Threshold voltage and charge separation for the 16Mb 5V/3.6V DRAM test structure..

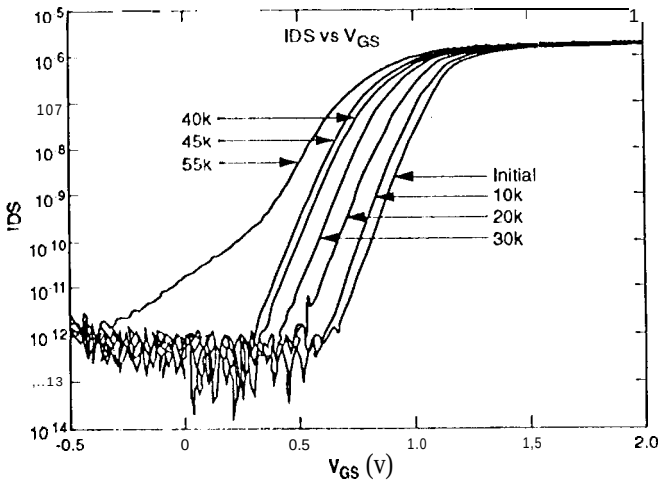

Figure 6. Subthreshold curves for the 16Mb 5V/3.6V DRAM test structure.